Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] What is claimed is:

1.A method for fabricating a trench capacitor of DRAM devices, comprising:

providing a substrate having a deep trench etched therein;

doping the deep trench to form a buried plate electrode in the substrate adjacent to a lower portion of the deep trench;

forming a node dielectric layer on interior surface of the deep trench;

depositing a first polysilicon layer in the deep trench;

recessing the first polysilicon layer to a first depth d_1 in the deep trench, a top surface of the recessed first polysilicon layer and the node dielectric layer constituting a first recess;

depositing a silicon spacer layer in the first recess;

anistropic etching the silicon spacer layer and the first polysilicon layer inside the deep trench to a second depth d_2, wherein the remaining silicon spacer layer becomes a spacer;

removing the node dielectric layer that is not covered by the spacer and the first polysilicon layer, thereby expos-

ing a silicon surface at a neck portion of the deep trench, wherein the node dielectric layer is divided into an upper dielectric section and a lower dielectric section that serves as a capacitor dielectric of the trench capacitor;

oxidizing the spacer, the silicon surface at the neck portion of the deep trench and an upper portion of the first polysilicon layer, thereby forming a silicon oxide layer; and

etching away the silicon oxide layer.

[c2] 2.The method of claim 1 wherein the substrate has a pad oxide layer and a pad nitride layer formed thereon.

[c3] 3.The method of claim 1 wherein the node dielectric layer is oxide-nitride-oxide (ONO) dielectric.

[c4] 4.The method of claim 1 wherein d_1 ranges between 200 and 500 angstroms.

[c5] 5.The method of claim 1 wherein d_2 ranges between 800 and 1500 angstroms.

[c6] 6.The method of claim 1 wherein the silicon spacer layer is made of amorphous silicon.

[c7] 7.The method of claim 6 wherein the silicon spacer layer has a thickness of about 200~350 angstroms.

[c8] 8.The method of claim 1 wherein after etching away the

silicon oxide layer, the method further comprises the following steps:

depositing a CVD oxide layer in the deep trench;

etching back the CVD oxide layer to form a collar oxide layer;

depositing a second polysilicon layer on the collar oxide layer in the deep trench;

recess etching the second polysilicon layer to a third depth d_3;

removing the collar oxide layer that is not covered by the second polysilicon layer; and

removing the upper dielectric section.

[c9] 9.The method of claim 8 wherein after removing the upper dielectric section, the method further comprises the following steps

depositing a third polysilicon layer atop the second polysilicon layer in the deep trench; and

recess etching the third polysilicon layer to a fourth depth d_4.